In The Specification:

Please amend the paragraph beginning at line 15 of page 11 as follows:

--[[~~switchFig.~~]]Fig. 3. is a diagram showing the connectivity of private output queues for controlling data congestion in a switch controller according to this invention. Each port of the switch controller of this invention has a private output queue. When a packet is received from one of the ports, the packet is sent to the private output queue. As shown in Fig. 3, the largest packet Ethernet capable of receiving is usually 1518 bytes (not including preamble and SFD columns). Hence, each buffer must have a size of at least 1.5KB. To request a buffer space, a signal is sent to a buffer control device so that a buffer is linked to the output queue. After the packet is forwarded and the storage space is emptied, linkage between the queue and the buffer is released and the associated buffer becomes free. For example, the queue in Fig. 3 is linked to four buffers.--

DLC 5-30-06

Please amend paragraph beginning at line 6 of page 18 as follows:

--Fig. 7 is a block diagram showing the connection of the switch controller of the Ethernet switching device according to this invention. As shown in Fig. 7, the Ethernet switching device 100 includes an switch controller 110, a static random access memory unit 120, a plurality of physical layer devices 130, an electrical erasable programmable read only memory (EEPROM) 140 and a central processing unit (CPU150). Size of the static random access memory unit 120 may [[~~bedetermined~~]]be determined by the jumpers. The controller 110 is coupled to the CPU150 port via a medium independent interface (MII). The controller 100 has a CPU port that couples with another CPU 150 port via an ISA/IDE interface line. In the meantime, the controller 110 is connected to a plurality of physical layer devices 130 through a reduced medium independent interface (RMII). RMII reduces pin out number so that the 14 pins of the MII can be reduced to just six.--

DLG 5-30-06

Please amend the paragraph beginning at line 17 of page 18 as follows:

--Fig. 8 is a block diagram showing the electrical connection of the switch controller according to this invention. As shown in Fig. 8, the switch controller 110 includes a plurality of port control devices 114, a queue control device 113, a forwarding control device 111 and a buffer control device 112. The plurality of port control deice 114 are coupled to the plurality of physical layer devices (PHY) 130 and a plurality of external signals. Through these physical layer devices 130, a plurality of state signals is received from the connection devices on the other end. These state signals include duplex mode and flow control capability signals. According to the flow control enable (Flow_Control_En) signal, the drop control enable (Drop_Conrol_En) signal and the backpressure enable (Backpressure_En) signal, the congestion control mechanism used by the switch controller 110 is selected. The flow control enable signal, the backpressure enable signal and the drop control enable signal can be determined by jumpers. The plurality of state signals generates a plurality of flow control window (XOFF_Window[9:0]) signals to the queue control device 113. According to the flow control window (XOFF_Window[9:0]) signals and the external signals, the selection of drop control is decided whether the drop-triggering signal DROP_ON[9:0] should [[beenabled]]be enabled.--